REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-21 remain in the application. Claims 1 and 12 have been amended.

Claim 1 has been amended by including the phrase --as a function of the associated bit--. The phrase "at least one of" has been deleted from claims 1 and 12, because the auxiliary register also needs to be stored. Similarly, claim 12 has been amended by adding the phrases --selecting registers of the register bank being stored as a function of their associated bits-- and --selecting the registers of the register bank storing data as a function of the associated bits--.

Support for these features can be found in line 15, page 19 to line to line 11 on page 20 of the instant specification in conjunction with Fig. 4 of the instant application.

In the second paragraph in item 3 on page 2 of the above-identified Office Action, claims 1-17 and 21 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner states that the claims are "incomplete for omitting essential structural cooperative relations of elements." Namely, "no functional relation has been recited with respect [to] the indication of the respective register containing the value with the stack buffer."

Regarding the rejection of claims 1 to 17, and 21 as being incomplete for omitting essential structural cooperative relationships of elements, applicants are not certain of the meaning of the Examiner's statements. The Examiner appears to require that the claims recite a connection between which registers are stored on the stack buffer. Applicants believe that the Examiner intended to state in the last sentence of the penultimate paragraph on page 2 of the Office Action that --no functional relation has been recited with respect to the indication of the respective register containing a value and between the stack buffer--. Accordingly, applicants have amended claims 1 and 12 to recite this relationship. If the Examiner meant otherwise, he is requested to clarify his statement so that applicants can address it.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, second paragraph. The above noted changes to the claims are provided solely for clarification or cosmetic reasons. The changes are not provided for overcoming the prior art nor do they narrow the scope of the claim for any reason.

In the fourth paragraph in item 3 on page 3 of the above-identified Office Action, claims 1-5, 9-12 14, and 15 have been rejected as being unpatentable over Chambers (U.S. 6,047,365) in view of Scheuneman (U.S. 4,757,440) in view of Fitch et al. (U.S. 5,056,060) (hereinafter "Fitch") under 35 U.S.C. § 103 (a).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is as noted above.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a microprocessor circuit, having:

at least one memory for free programming with at least one program having functions, the memory connected to a control unit;

a register bank having registers, the register bank connected to the control unit;

an auxiliary register storing a number of bits, each of the bits being associated with one of the registers of the register bank and indicating whether a respective one of the registers contains a value different from a logical "0", the auxiliary register connected to at least one of the control unit or the register bank, and **a stack for buffer-storing data of the auxiliary register as a function of the associated bit, of the registers of the register bank, the stack connected to at least one of the control unit, the register bank, or the auxiliary register.** (emphasis added)

Applicants respectfully disagree with the Examiner's rejection of claim 1 over Chambers in view of Scheuneman in view of Fitch.

Chambers does not disclose both a memory for free programming and a stack for buffer storing data of the auxiliary register and the registers of the register bank as recited in claims 1

and 12 of the instant application.

In Chambers, the sample pages 306 of Figure 3 are part of the system memory and are not a stack...they are a page. A stack is characterized in that data is added or removed in a last in, first out manner. As such it is a very simple process and no memory management unit (MMU) is required. Further, the order of the data elements is preserved which is important in the present invention for the correct storing and rereading registers of the register bank in the stack. By comparison, Chambers' paging is a memory allocation algorithm in which the memory is divided into small portions which do not need to be contiguous and can be randomly addressed. Further, for paging a complicated addressing scheme for the memory is necessary as shown by the elements drawn to the left of the system memory 306 used for the sample page in Figure 3 of Chambers. The Examiner's argument that the sample page 306 is connected to at least the control unit, the register bank, the auxiliary register and therefore has storage capabilities does not make it into a stack as set forth in the instant claims. Therefore, applicants submit that Chambers does not disclose a stack as recited in claims 1 and 12 of the instant application.

Further, the sample pages 306 of Chambers are not used for

storing data of the auxiliary registers and the registers of the register bank. The output of the adder 324 is a 32-bit address which is only used to address one of the sample pages but is not stored in the sample pages 306. In contrast, claims 1 and 12 recite that data from the auxiliary registers and the registers of the register bank are stored in the stack.

Therefore, it is apparent that Chambers does not show several claimed features of the instant invention and moreover, does not show the claimed feature that storing of the registers of the register bank depends on the associated bits.

Scheuneman discloses a digital data processing system having a virtual stack structure which incorporates a plurality of stack registers. Each register has a unique write tag and read tag associated with it. Chambers does not use or disclose the term "stack". Therefore, there is no suggestion, motivation, or reason to look to Scheuneman which discloses a system including a stack buffer. Chambers and Scheuneman relate to different technical fields. It is apparent that the Examiner relies on hindsight and knowledge of the instant invention in order to find a basis for combining Chambers and Scheuneman. The Examiner's reasoning that the stack buffer of Scheuneman should be combined with Chamber to increase the

storage capacity is incorrect and not logical, since a limitation of storage capacity is not addressed as a concern or problem by Chambers. The Examiner states that "one of ordinary skill in the art should be able to recognize the stack of Scheuneman with the read/write tags could be used for Chambers' stack". However, this conclusion is incorrect because there is no motivation or suggestion in Chambers to warrant or justify such a combination of references as proposed by the Examiner.

Fitch discloses a printed circuit card board card having a self-configuring memory system for allocation of reserved memory space among expansion cards. Fitch does not make up for the deficiencies of Chambers and Scheuneman.

Applicants submit that claim 1 is not obvious over Chambers in view of Scheuneman and Fitch. The same arguments apply to claim 12.

In item 12 on page 6 of the above-identified Office Action, claims 6, 7, and 8 have been rejected as being unpatentable over Chambers in view of Scheuneman in view of Fitch and further in view of Arnold et al. (U.S. 4,558,176) (hereinafter "Arnold") under 35 U.S.C. § 103 (a).

Regarding claims 6 to 8, neither Chamber, Scheuneman, Fitch nor Arnold disclose the second stack as recited in the instant claims. Chambers does not provide any motivation or suggestion to use a read only memory as alleged by the Examiner on page 7, first paragraph, of the above-identified Office Action. Chambers in column 1, lines 16 to 32, discloses that a dedicated ROM is not always cost-effective and that if system memory can be used for storing wave table samples, it can then be used for another purpose at a different time (see column 1, lines 34 to 47). In fact, Chambers uses a dynamic RAM which is both readable and writable without restriction and is not needed if a dedicated ROM is used, as there is no need to access the PC I-bus. Therefore, it is apparent that Chambers does not suggest or show using a read only memory but instead promotes using a RAM system memory. Consequently, Chambers does not contain any suggestion or reason to rely on Arnold to modify Chambers to include an inaccessible stack. Furthermore, Chambers does not disclose anything about or relating to security, so that the Examiner's statement that Arnold could provide Chambers with the ability to protect the content of this stack is again based on hindsight. Alternatively to being patentable as a dependent claim on claim 1, which is deemed patentable for the reasons advanced above, claim 6 is therefore considered patentable per se.

In item 14 on page 7 of the above-identified Office Action, claims 13, 16, and 17 have been rejected as being unpatentable over Chambers in view of Scheuneman in view of Fitch and further in view of Wright et al. (U.S. 4,802,218) (hereinafter "Wright") under 35 U.S.C. § 103 (a).

Applicants presume that the Examiner did not intend to reject claims 16 and 17 because the Examiner has stated that claims 16 and 17 would be allowable if rewritten to be independent.

The same arguments for patentability of claims 6 to 8 also apply equally to claim 13. The Examiner argues that Chambers teaches a read only memory. Chambers does not teach a read only memory so that there is no motivation or reason to store a register of the register bank only on a stack if the associated auxiliary register has a value different from the logical "0".

Chambers does not show "a stack for buffer-storing data of said auxiliary register and, as a function of the associated bit, of said registers of said register bank, said stack connected to at least one of said control unit, said register bank, or said auxiliary register" as recited in claim 1 of the instant application, or "storing data being stored in the auxiliary register and the registers of the register bank in

the stack, selecting registers of the register bank being stored as a function of their associated bits, or storing data being stored in the stack in the auxiliary register and in the registers of the register bank, and selecting the registers of the register bank storing data as a function of the associated bits" as recited in claim 12 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1 or 12. Claims 1 and 12 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 12.

Finally, applicants appreciatively acknowledge the Examiner's statement that claims 16-20 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." In light of the above, applicants respectfully believe that rewriting of claims 16-20 is unnecessary at this time.

In view of the foregoing, reconsideration and allowance of claims 1-21 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time is required for this paper, petition for extension is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer, LLP, No. 12-1099.

Respectfully submitted,

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FDP/am

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